What is claimed is:

1. A differential output circuit comprising:

a first input receiving a first input signal;

a second input receiving a second input signal complementary to said first input signal;

first and second outputs;

a resistor element connected between said first and second outputs;

a first N-channel MISFET having a source connected to said first input, a gate receiving a power supply potential, and a drain connected to said first output;

a second N-channel MISFET having a source connected to said second input, a gate receiving said power supply potential, and a drain connected to said second output;

a first P-channel MISFET having a source receiving said power supply potential, a gate connected to said second input, and a drain connected to said first output; and

a second P-channel MISFET having a source receiving said power supply potential, a gate connected to said first input, and a drain connected to said second output.

2. The differential output circuit according

to claim 1, further comprising an inductive element, wherein said resistive element and said inductive element are connected in series between said first and second outputs.

3. The differential output circuit according to claim 2, wherein said inductive element includes first and second inductors having a substantially same inductance, said first inductor being connected between one terminal of said resistive element and said first output, and said second inductor being connected between another terminal of said resistive element.

4. The differential output circuit according to claim 2, wherein said resistive element includes first and second resistors having a substantially same resistance, said first resistor being connected between one terminal of said inductive element and said first output, and said second resistor being connected between another terminal of said inductive element.

5. A differential output circuit comprising:

a first input receiving a first input signal;

a second input receiving a second input

signal complementary to said first input signal;

an output circuit developing first and second complementary output signals on first and second outputs in response to said first and second input signals, respectively; and

an inductive element connected between said first and second outputs.

6. The differential output circuit according to claim 5, wherein said output circuit includes:

a first N-channel MISFET having a source connected to said first input, a gate receiving a power supply potential, and a drain connected to said first output,

a second N-channel MISFET having a source connected to said second input, a gate receiving said power supply potential, and a drain connected to said second output,

a first P-channel MISFET having a source receiving said power supply potential, a gate connected to said second input, and a drain connected to said first output, and

a second P-channel MISFET having a source receiving said power supply potential, a gate connected to said first input, and a drain connected to said second output.

7. An integrated circuit comprising:

a logic circuit developing first and second clock signals complementary to each other; and

a differential output circuit responsive to said first and second clock signals to develop first and second complementary output signals on first and second outputs, respectively,

wherein said differential output circuit includes an inductive element connected between said first and second outputs.

8. The integrated circuit according to claim 7, wherein said differential output circuit further includes:

first and second inputs receiving said first and second clock signals, respectively,

a first N-channel MISFET having a source connected to said first input, a gate receiving a power supply potential, and a drain connected to said first output,

a second N-channel MISFET having a source connected to said second input, a gate receiving said power supply potential, and a drain connected to said second output,

a first P-channel MISFET having a source receiving said power supply potential, a gate connected to said second input, and a drain

connected to said first output, and

a second P-channel MISFET having a source receiving said power supply potential, a gate connected to said first input, and a drain connected to said second output.

9. An integrated circuit comprising:

a logic circuit developing first and second sinusoidal signals whose phases are different by 180 degrees; and

a differential output circuit responsive to said first and second sinusoidal signals to develop first and second complementary output signals on first and second outputs, respectively,

wherein said differential output circuit includes an inductive element connected between said first and second outputs.

10. The integrated circuit according to claim 9, wherein said differential output circuit further includes:

first and second inputs receiving said first and second sinusoidal signals, respectively,

a first N-channel MISFET having a source connected to said first input, a gate receiving a

power supply potential, and a drain connected to said first output,

a second N-channel MISFET having a source connected to said second input, a gate receiving said power supply potential, and a drain connected to said second output,

a first P-channel MISFET having a source receiving said power supply potential, a gate connected to said second input, and a drain connected to said first output, and

a second P-channel MISFET having a source receiving said power supply potential, a gate connected to said first input, and a drain connected to said second output.

11. An integrated circuit comprising:

a logic circuit developing first and second input signals complementary to each other, wherein said logic circuit includes:

a first pull-up N-channel MISFET used for pull-up of said first input signal, and

a second pull-up N-channel MISFET used for pull-up of said second input signal; and

a differential output circuit including:

a first input receiving said first input signal;

a second input receiving said second

input signal;

first and second outputs;

a resistor element connected between said first and second outputs;

a first N-channel MISFET having a source connected to said first input, a gate receiving a power supply potential, and a drain connected to said first output;

a second N-channel MISFET having a source connected to said second input, a gate receiving said power supply potential, and a drain connected to said second output;

a first P-channel MISFET having a source receiving said power supply potential, a gate connected to said second input, and a drain connected to said first output; and

a second P-channel MISFET having a source receiving said power supply potential, a gate connected to said first input, and a drain connected to said second output.

12. The integrated circuit according to claim 11, further comprising an inductive element, wherein said resistive element and said inductive element are connected in series between said first and second outputs.

13. An integrated circuit comprising:

a logic circuit developing first and second input signals complementary to each other, wherein said logic circuit includes:

a first pull-up N-channel MISFET used for pull-up of said first input signal, and

a second pull-up N-channel MISFET used for pull-up of said second input signal; and

a differential output circuit including:

a first input receiving said first input signal;

a second input receiving said second input signal;

first and second outputs;

an inductive element connected between said first and second outputs;

a first N-channel MISFET having a source connected to said first input, a gate receiving a power supply potential, and a drain connected to said first output;

a second N-channel MISFET having a source connected to said second input, a gate receiving said power supply potential, and a drain connected to said second output;

a first P-channel MISFET having a source receiving said power supply potential, a gate connected to said second input, and a drain

connected to said first output; and

a second P-channel MISFET having a source receiving said power supply potential, a gate connected to said first input, and a drain connected to said second output.